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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/677,158	10/01/2003	Ming-Fang Wang	67,200-1160	8159

7590 10/02/2006

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EXAMINER	
GEORGE, PATRICIA ANN	

ART UNIT	PAPER NUMBER
1765	

DATE MAILED: 10/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/677,158	WANG ET AL.	
	Examiner	Art Unit	
	Patricia A. George	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *31 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9,11 and 13-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,11 and 13-22* is/are rejected.

7)☒ Claim(s) *9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Finality has been withdrawn.

The remarks filed 8/31/2006 is sufficient to overcome the grounds of rejection filed 5/18/2006 based upon an improper use of the Labelle et al reference, as the filing date is after applicants' instant application. Examiner would like to both thank applicant for pointing out this error, and apologies for any incontinence this oversight caused. A new ground of rejection is offered below.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
>
> This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1, 9, 19, and 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Guo. (6,596,599) in view of Hsiao et al. (2004/0241920), evidenced by Intel (Intel: Glossary for Intel's High K, Metal Gate Transistor Announcement).

As to claim 1, Guo teaches a method of forming a high-K dielectric stacked gate structure (fig. 4, parts 52, & 54) over a semiconductor substrate (10); a gate electrode

(see figures 4-14) over the high-K dielectric stacked gate structure, by means of lithography patterning (see description of fig. 3) and etching (see description of fig. 4); to achieve the prevention of excessive gate leakage current from occurring the vertical field between the gate structure and the channel region of the gate is maximized by the high-k gate dielectric, minimizing capacitive coupling between the source/drain regions of the structure and the gate electrode (i.e. reduces interface states between a high-k dielectric and a gate electrode) (see abstract). Further evidence of the reduction of interface states between a high-k dielectric and a gate electrode is offered by Intel, who teaches by definition use of High-k-material greatly reduces leakage (i.e. reduces interface states between a high-k dielectric and a gate electrode).

Guo fails to teach a step of plasma treatment of the gate structure, using a gas as applicants limitation in claim 1, 9, and 19.

Hsiao et al. teaches a method of H.sub.2 plasma treatment (as in claims 1, 9, and 19) of gate metal (see abstract).

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to include a step of H.sub.2 plasma treatment, as Hsiao et al., when forming a high-K dielectric stacked gate structure, as Guo, because Hsaio ewt al. teaches it will improve: the adhesion of the gate insulating film on the gate metal, the electrical characteristics of the gate insulating film, the resistivity of the thin film transistor source and drain regions, and improve the stress characteristics of the thin film transistor (see para. 10).

Claim Rejections - 35 USC § 103

Claims 2-4, 13-15, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Guo and Hsiao et al. (herein referred to as Hsiao), as applied to claim 1, 9, 19, and 21 above, further in view of both Teng et al. (6,797,576) and Wolf Wolf (Silicon Processing for the VLSI Era, Volume 1; Process Technology; pg.58, para. 2, 1986 Latice Press; ISBN 0-9616721-3-7).

The modified teaching of Guo fails to teach the limitations presented in claims 2-4, 13-15, and 22.

As to claims 2, 13, and 22, Teng teaches a step of annealing the gate electrode structure (as in claims 2, 13, and 22), at 525 degrees C. to 1100 degrees C. which encompasses applicants range of 600 to 750 degree C (as in claims 3, and 14), in an ambient of nitrogen (as in claim 4, and 15) (see col. 51, lines 10-36).

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to include the step of annealing, as Teng et al., when forming a high-K dielectric stacked gate structure, as Guo, because Teng et al. teaches the anneal will repair lattice damage and activate the implanted source/drain and halo dopants.

With respect to claims 3-4, and 14-15 Wolf also teaches it is desirable to use N2 ambient for annealing (as in claims 4 and 15), carried out from 420-1150 degree.C (which encompasses applicants' range in claims 3 and 14).

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to modify the invention of annealing after forming and treating the

gate structure (para. 0016), as Guo., by including the temperature range and N2 ambient, as Wolf, because Wolf teaches it is known and a desirable option of annealing.

Claim Rejections - 35 USC § 103

Claims 5, 7, 16, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Guo and Hsiao et al. (herein referred to as Hsiao), as applied to claim 1, 9, 19, and 21 above, further in view of Shinriki et al. (2005/0074983).

The modified teaching of Guo is silent as to the base dielectric layer of the gate stack comprising SiO.sub.2, as in claims 5.

Shinriki et al. teaches it is preferably to change the composition of the dielectric stack gradually from the SiO.sub.2 base to a composition primarily of high-k dielectric, metal oxides such as hafnium oxide (see para. 83) as to avoid defects such as interface states (see para. 0006), as in claims 5, 7, 16, and 18.

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to modify the teaching of a dielectric stack layer, as in Guo, to include that the base comprise SiO.sub.2, under hafnium oxide, as in Shinriki et al., because Shinriki et al. teaches it is preferable because it avoids defects such as interface states (see para. 0006).

Claim Rejections - 35 USC § 103

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Guo and Hsiao et al. (herein referred to as Hsiao), as applied to claim 1, 9, 19, and 21 above, further in view of Haukka et al. (2002/0115252).

Guo is silent as to the materials listed in claim 6, being high-k.

Haukka et al. teaches it is known that high-k materials comprise all the materials as claimed by applicants' in claim 6 (see para. 7).

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to include the high-k materials, as listed by applicatnts, when forming a stacked gate structure of high-K dielectric materials, as Guo, because Haukka et al. teaches it is known that claimed materials are high-K dielectrics, and Guo teaches process improvement result as an effect of using high-K materials.

Claim Rejections - 35 USC § 103

Claim 8 rejected under 35 U.S.C. 103(a) as being unpatentable over the modified invention of Guo, Hsiao and Shinriki, as applied to claims 5, 7, 16, and 18 above, and further in view of Sarigiannis et al. of 2004/0152304.

As to claim 8, the modified invention of Guo is silent as to how the high-k dielectric materials may be formed, such as ALD (ALCVD) at less than 300 degree C, as in claim 8.

Sarigiannis et al.teaches an ALD deposition temperature of 200 degree C, (para.4, l.11), which is within the claimed range of less than about 300 degree C".

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to include a process temperature for ALD deposition, as Sarigiannis, when forming the gate structure, of Guo, because Sarigiannis teaches it can be advantageous.

Claim Rejections - 35 USC § 103

Claims 11 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Guo, Hsiao and Shinriki, as applied to claims 1-2, 4, 6, and 9 above, further in view of Steger (5,085,727).

As for claim 11, Guo. teaches a plasma etcher may be used for the treatment process, however the modified teaching of Guo is silent as to the pressure of the plasma treatment, as applicants' claim.

Steger teaches plasma etcher can operate in a range of between about 1 mTorr to about several Torr which is dependant on the type of plasma system used, (see col. 5, lines 31-39) and encompasses applicants' claimed range of about 100 mTorr to about 10 Torr.

It would have been obvious to one of ordinary skill in the art at the time of invention was made, to modify the invention of Guo to include the pressure ranges, as in Steger, because Steger teaches plasma etchers can be used at the specific pressures as applicants' limitations in claim 11 and 20, are known to be effective. Since the reference of Steger does not limit the pressure range selected, one of ordinary skill would use a plasma etcher for the method of plasma treatment at any desired pressure, including applicants specifically claimed range.

Response to Arguments

Applicant's arguments filed 5/18/06 have been fully considered and are persuasive, see response to amendments above.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: US 2003/0124824.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Patricia A. George whose telephone number is (571)272-5955. The examiner can normally be reached on weekdays between 7:00am and 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on (571)272-1465. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Patricia A George
Examiner
Art Unit 1765

PAG
09/06

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SUPERVISORY PATENT EXAMINER
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